Cadence Encounter Test User Guide

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Cadence Encounter Test User Guide

Starting Encounter • To start the tool, first you must source the environment file source set_cadence_soc_env <CR> –This file sets up the paths and license file access to run First Encounter • Then on the command line type encounter <CR>

Cadence First Encounter Tutorial

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In this tutorial you will gain experience using Cadence Encounter to perform automatic placement and routing. A place+route tool takes a gate-level netlist as input and first determines how each gate should be placed on the chip.

Automatic Placement and Routing using Cadence Encounter

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA. Product Encounter™ RTL Compiler contains technology licensed from, and copyrighted by: Concept Engineering GmbH, and is 1998-2006, Concept Engineering GmbH.

Command Reference for Encounter RTL Compiler

Encounter User Guide May 2008 4 Product Version 7.1.2 Using Text Command Help 58

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Tutorial for Encounter. Tutorial for Encounter. STEP 1: Login to the Linux system on Linuxlab server. Start a terminal (the shell prompt). (If you don’t know how to login to Linuxlab server. , look at here) Click here to open a shell window. Fig. 1 The screen when you login to the Linuxlab through equeue. STEP 2: Build work environment for class ESE461.

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Cadence® custom, analog, and RF design solutions can help you save time by automating many routine tasks, from block-level and mixed-signal simulation to routing and library characterization. ... “I successfully learned how to deploy Encounter Test for the various DFT-SCAN preparation checks and SCAN-chain insertion tasks. It was helpful to ...

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window. Type “test_cm” on Name field, click Add button in “SDC Constraint Files” tab which opens “Timing Library Files” window. f) In the “SDC Constraint Files” window, expand the window by clicking “>>”, and double-click test.sdc, and close the window.

Tutorial I: Cadence Innovus
Summary of Contents for Cadence ENCOUNTER CONFORMAL EQUIVALENCE CHECKER. Page 1 ENCOU N TE R C O N FOR MA L EQUIVA LE N C E C H EC K ER Cadence Encounter Conformal Equivalence Checker (EC), ® ® ® makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the only complete equivalence checking solution available for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs.

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